REMARKS

Claim 12 is pending.

Claim 12 was rejected under 35 USC 103(a) as being unpatentable over Applicant's admitted prior art (Fig. 9) in view of Hu, U.S. Patent 5,780,899, Tsui, U.S. Patent 5,960,289, and Hodges, "Analysis and design of digital integrated circuits". This rejection is respectfully traversed.

Claim 12 recites "first MOS transistors operating at the first voltage and second MOS transistors operating at a second voltage higher than the first voltage and performing direct signal transmission and reception to and from an external device, said first MOS transistors each have a channel-forming semiconductor region formed of a first well, and said second MOS transistors each have a channel-forming semiconductor region formed of a second well deeper than the first well." Neither Applicant's own Fig. 9, Hu, Tsui or Hodges, alone or in combination, teach or suggest these features. Further, the Examiner never actually alleges that any of these references actually teaches the claimed features quoted above.

The Examiner asserts that Hu shows a DTMOS device that has an n-well deeper than the p-well, but never asserts that Hu teaches first MOS transistors operating at a first voltage and second MOS transistors operating at a second voltage higher than the first voltage. The Examiner also never asserts that Hu teaches that the first MOS transistors each have a channel-forming semiconductor region formed of a first well and the second MOS transistors each have a channel-forming semiconductor region formed of a second well that is deeper than the first well. In fact, Hu is actually directed to different trench isolation schemes such as those shown in Figs. 6, 7 and 8. Each of these embodiments do show a deep n-well with a shallow p-well formed in the deep n-well, but Hu is totally silent with respect to the operating voltages of the transistors and certainly never discloses that first MOS transistors having a first well operate a lower voltage than the second MOS transistors which have a second well which is deeper than the first well. Rather, as stated above, the Examiner merely alleges that Hu teaches an n-well deeper than a p-well, which is not what is being claimed. Hodges and Tsui likewise fail to teach or suggest the above-quoted features of claim 12.

Thus, even if the cited references were combined, the combination would fail to teach or suggest the features of claim 12.

Furthermore, Applicant respectfully submits that the Examiner is relying on impermissible hindsight in this rejection.

According to the claimed invention, the first well and the second well have different depths and each of the second MOS transistors, which operate at a higher voltage and perform direct signal transmission and reception to and from an external device, has a channel-forming semiconductor region made of the deeper, second well. The purpose of this particular arrangement is to improve reliability in terms of the electrostatic withstand voltage (see pg. 8, lines 5-7).

The Examiner merely asserts that the motivation for combining the cited references as being "for the advantages shown." The Examiner's alleged motivation is so general in the context of the relevant art as to constitute no more than the reference to a general level of skill in the art found deficient in *In re Lee*, 277 F.3d 1338, 1343, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002). Under *Lee*, the Examiner must present *specific* evidence of motivation, not the kind of generalized allegation of motivation relied on in the pending Action:

> When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness. *See, e.g., McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001) ("the central question is whether there is reason to combine [the] references," a question of fact drawing on the *Graham* factors).

The burden imposed by *Lee* is not an impossible burden, as explained by the court in *In re Thrift*, 298 F.3d 1357, 1364-65, 63 USPQ2d 2002, 2007 (Fed. Cir. 2002), with respect to the references relied on by the Board in that case:

> In the present case, the reasoning articulated by the Board is exactly the type of reasoning required by *In re Lee*. Both the examiner and the Board clearly identified a motivation to combine the references, stating that the skilled artisan would have "found it obvious to incorporate the speech input and speech recognition techniques taught by Schmandt into the expert system of Stefanopoulos in order to reduce the need for less user friendly manual keyboard and mouse click inputs." Decision on Appeal at 5; accord Aug. 7, 1996 Office Action at 3. The motivation to combine the references is present in the text of each reference. The Schmandt reference itself verifies this motivation, stating that "allowing users to remain focused on the screen and keyboard, instead of fumbling for the mouse, would be beneficial in a workstation environment." Schmandt at 51. Stefanopoulos itself, while not expressly disclosing the use of speech recognition, sets forth the motivation to combine the references, stating that "there are alternative means to select the buttons, including . . . voice-activated transfer means, which may be readily adapted for use with the present invention by those skilled in the art." '237 patent, col. 4, ll. 34-38.

The reliance in the pending Action comes nowhere close to what *Lee* and *Thrift* require. It is not sufficient to say without evidentiary support, as the Examiner does in the pending Action, that the motivation for modifying the prior art is "for the advantages shown."

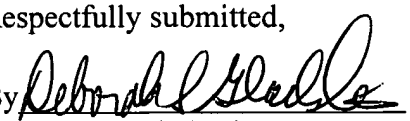
Furthermore, Hu fails to teach reasons why the p- and n-wells for forming the n- and p-MOS devices are made to have different depths or any advantages/effects brought by such a dual well depth arrangement. Thus, one of ordinary skill in the art would not have been motivated to combine Tsui's transistors operating at different voltages with the p- and n-wells that are of different depths in Hu. Thus, there would have been no motivation to combine the references as asserted by the Examiner and the Examiner is merely using impermissible hindsight in an effort to recreate the claimed invention. Accordingly, Applicant requests that this rejection be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no. 204552016501.

Dated: August 12, 2005

Respectfully submitted,

By 

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